

FORM PTO-1449 (modified)
To: U.S. Department of Commerce
(PW FORM PAT-1449)
Patent and Trademark Office

Atty.
Dkt. No.

M#

Client Ref.

284163

01F181

Applicant: INABA

Appln. No.:

Filing Date: Herewith

Examiner:

Group Art Unit:

**INFORMATION DISCLOSURE STATEMENT
BY APPLICANT**

Date: January 11, 2002

Page

1

of

1

U.S. PATENT DOCUMENTS

Examiner's Initials*		Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
TD	AR	5,675,172	10/1997	MIYAMOTO et al.			
	BR						
	CR						
	DR						
	ER						
	FR						
	GR						
	HR						
	IR						
	JR						
	KR						
	LR						
	MR						
	NR						

FOREIGN PATENT DOCUMENTS

		Document Number	Date MM/YYYY	Country	Inventor Name		English Abstract	Translation Readily Available
							Enclosed	No
	OR							
	PR							
	QR							
	RR							
	SR							
	TR							
	UR							
	VR							
	WR							
	XR							

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

TD	YR	M. Miyamoto, R. Nagi and T. Nagano, "Pseudo-SOI: P-N-P Channel-Doped Bulk MOSFET for Low-Voltage High Performance Applications, IEDM 1998, pp. 411-414			
TD	ZR	T. Mizuno, Y. Asao, J. Koga, "High Performance Shallow Junction Well Transistor (SJET)", ULSI Resarch Center, pp. 109-110			
	AAR				
	BBR				
	CCR				
	DDR				

Examiner

Date Considered:

10/19/02